Digital Logic Design Laboratory

Lab 3

MSI Combinational Logic (II)

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Class: ……………………………………………….......

Date: …………………………………………………....

# I. Objectives

In this laboratory, students will study:

- Understand the operation of combinational logic circuit.

- The operation of some combinational ICs such as: full adder, decoder, encoder.

# II. Procedure

1. Design the adder with two one-bit binary.

a. Design the half adder two one-bit binary.

Two inputs are A, B. Two outputs are S and C.

Build the truth table and the expressions

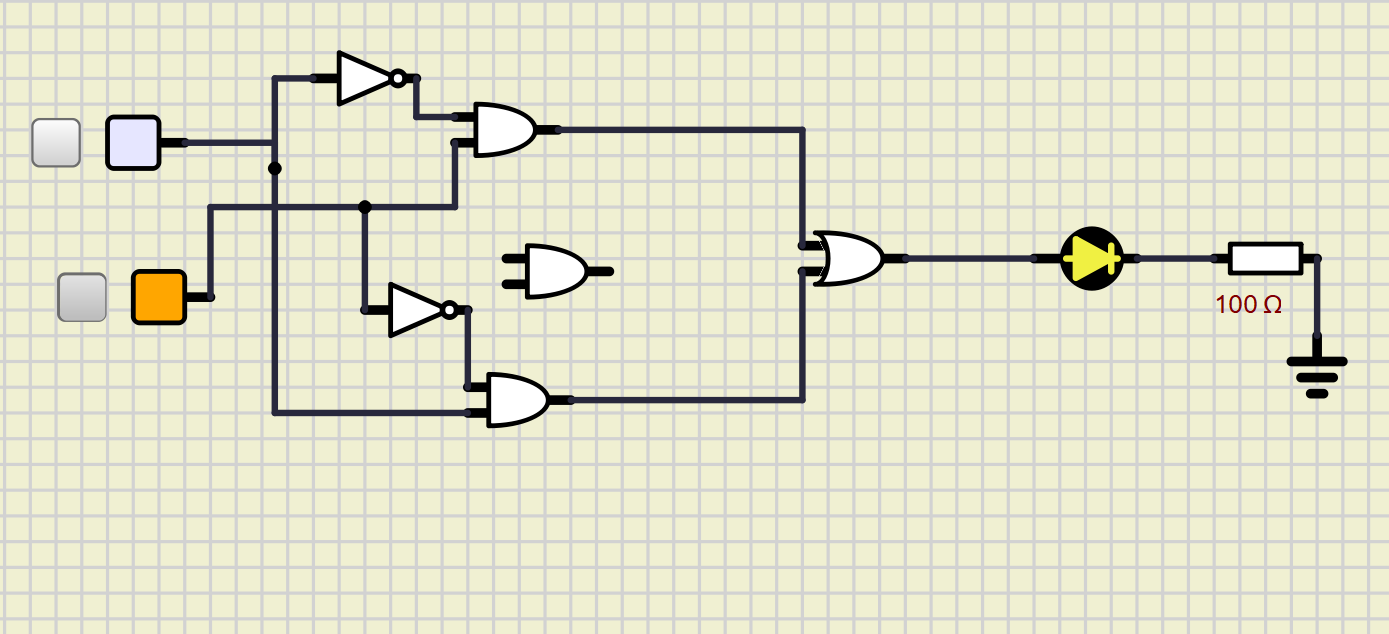
|  |  |  |  |
| --- | --- | --- | --- |
| A | B | S |  |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 |

The simplified expressions:

S =

C = AB

Implement the circuit via simulation software and paste the result in here



Case 2:

A diagram of a circuit

Description automatically generated

Case 3:

A diagram of a circuit

Description automatically generated

Make comment on the results

b. Design the full adder two one-bit binary.

Three inputs are Cin, A, B. Two outputs are S and Cout.

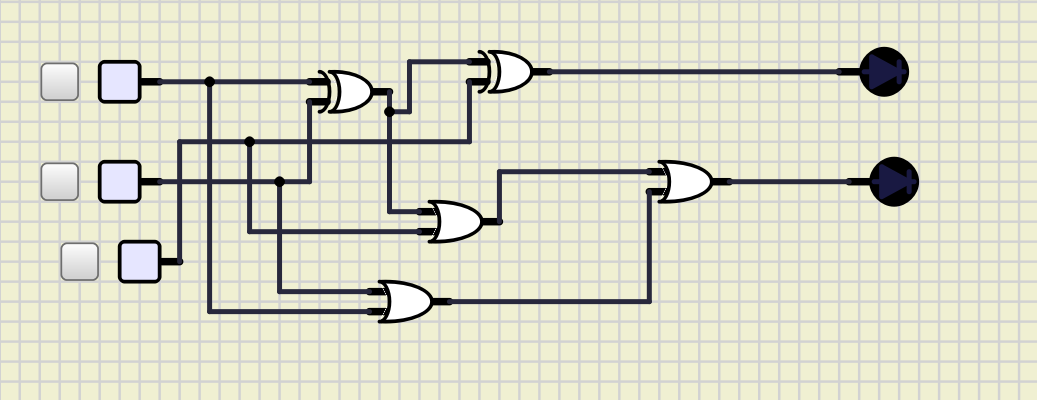
Build the truth table and the expressions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B |  | S |  |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

The simplified expressions:

|  |  |  |
| --- | --- | --- |
|  | 0 | 1 |
| 00 | 0 | 0 |
| 01 | 0 | 1 |
| 11 | 1 | 1 |
| 10 | 0 | 1 |

Implement the circuit via simulation software and paste the result in here



A diagram of a circuit

Description automatically generated

A diagram of a circuit

Description automatically generated

Make comment on the results

2. 8-to-3 Priority Encoder (Interrupt sorter) – IC 74HC148

a. Investigate IC – 74HC148

Construct the circuit as below:

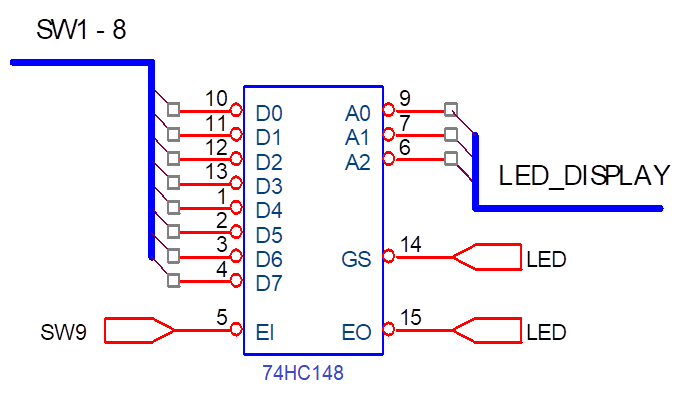


Figure 1 – Encoder 8-to-3 IC 74LS148

- The outputs are connected to LED displays to determine the logic levels.

- Choose the input data D0 - D7 by switches in the order from SW0 to SW7.

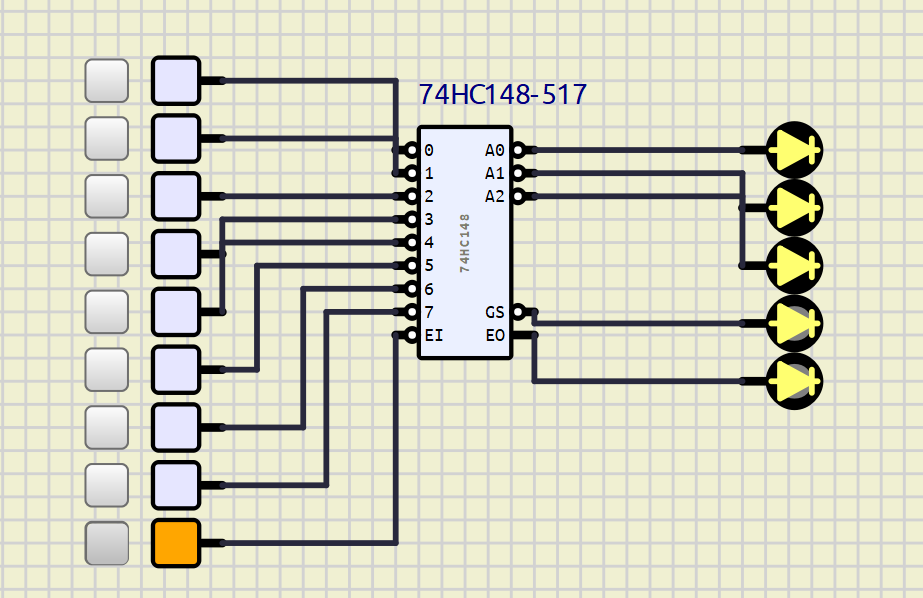
- Control EI by using switch.

- Observe the results and fulfill the truth table of 74HC148.

- What are the functions of  and ?

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | | | | | | | | | Output | | | | |
| EI | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | GS | A2 | A1 | A0 | E0 |
| 1 | X | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | X | X | X | X | X | X | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | X | X | X | X | X | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | X | X | X | X | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | X | X | X | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

Implement the circuit via simulation software and paste the result in here



A computer circuit board with many wires

Description automatically generated

b. Priority encoder

Let’s EI equal to 0, fill the outputs A2, A1, A0 in the following cases

|  |  |  |  |
| --- | --- | --- | --- |
|  | A2 | A1 | A0 |
| Case 1:  I3 = I2 = I1 = 0  I7 = I6 = I5 = I4 = I0 = 1. | 1 | 0 | 0 |
| Case 2:  I7 = I2 = 0.  I6 = I5 = I4 = I3 = I1= I0 =1 | 0 | 0 | 0 |
| Case 3:  All 8 inputs are equal to 0. | 0 | 0 | 0 |

Case 1:

Implement the circuit via simulation software and paste the result in here

A computer diagram of a circuit board

Description automatically generated

Make comment on results

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Case 2:

Implement the circuit via simulation software and paste the result in here

A circuit board with many wires

Description automatically generated

Make comment on results

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Case 3:

Implement the circuit via simulation software and paste the result in here

A computer circuit diagram with many black wires

Description automatically generated with medium confidence

Make comment on results

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

3. 2-to-4 Decoder - IC74HC139

Construct the circuit as below:

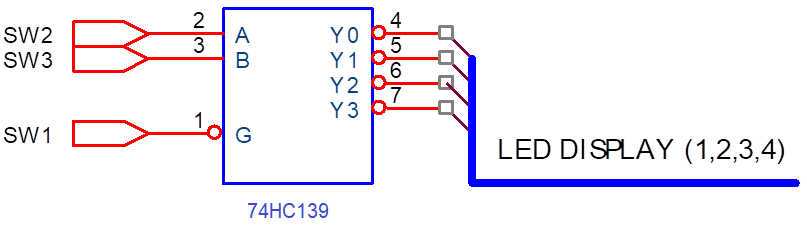


Figure 2 – Decoder 2-line-to-4-line IC 74HC139

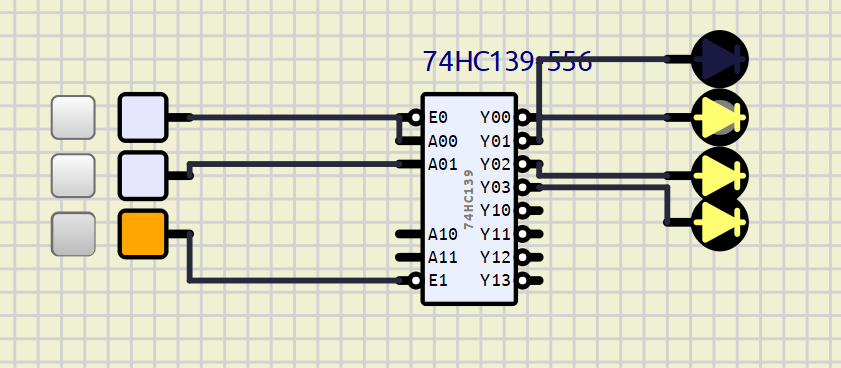
- 4 outputs (Y0-Y3) are connected to LED display (Led 1-4).

- The data inputs (A, B) and control input (G) are connected to switches.

- Change the states of inputs to fulfill the truth table of IC 74HC139.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | Outputs | | | |
| Control | Data | |
| G | B | A | Y0 | Y1 | Y2 | Y3 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | X | X | 1 | 1 | 1 | 1 |

Implement the circuit via simulation software and paste the result in here



A computer circuit board with wires

Description automatically generated

Briefly describe the operation of the IC

4. 3-TO-8 Decoder– IC 74HC138

Construct the circuit as below:

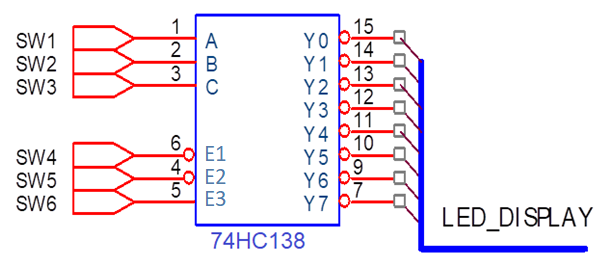


Figure 3 – 3-to-8 Decoder/demultiplexer - IC 74HC138

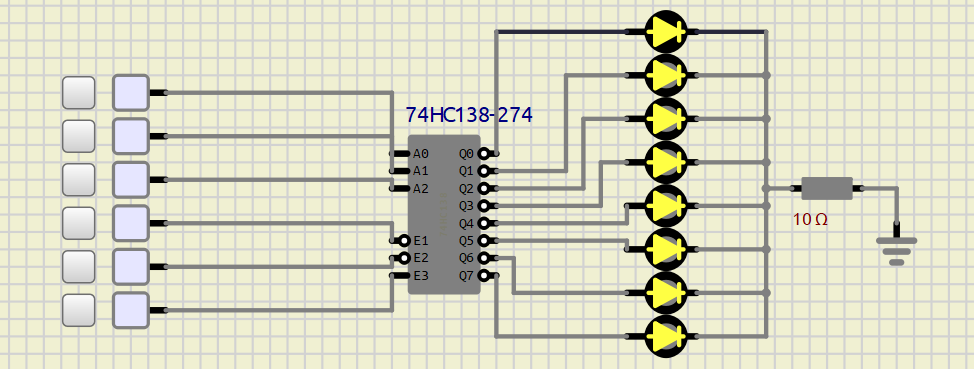
- 8 outputs are connected by using LEDs.

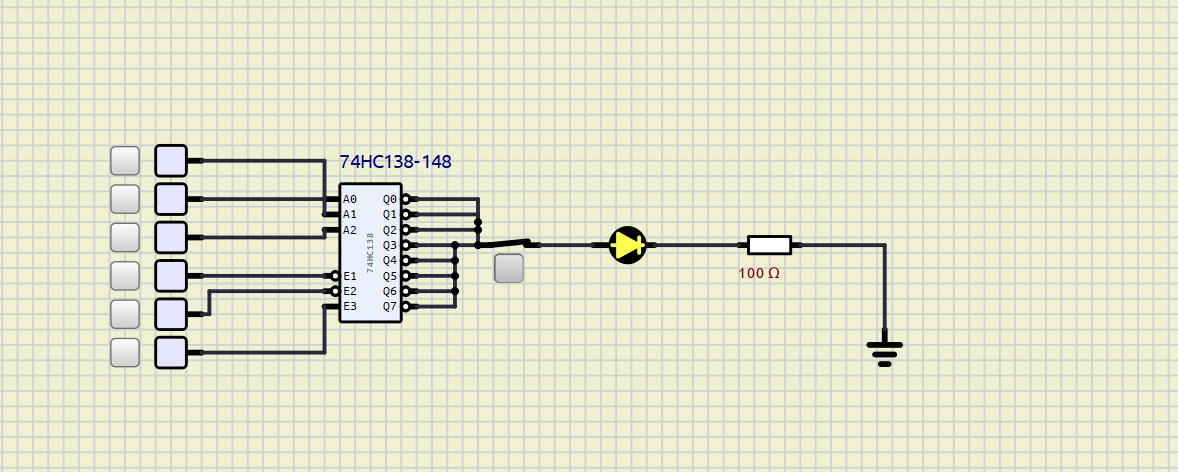
- The inputs are controlled by switches.

- Observe the results and fulfill the truth table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| INPUT | | | | | | OUTPUT | | | | | | | |
| E3 | E2 | E1 | C | B | A | Y0 | Y1 | Y2 | Y 3 | Y4 | Y 5 | Y 6 | Y7 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | 1 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | 1 | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Implement the circuit via simulation software and paste the result in here





Briefly describe the operation of the IC

5. Design combinational circuits using decoders and OR gate

- Implement Boolean expression using IC 74HC138 & OR gate.

- The data inputs A, B, C are connected to switches.

- The control inputs are in suitable levels.

- Implement the circuit and verify the truth table

a.

Establish the truth table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| X | Y | Z | F | Num |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 2 |
| 0 | 1 | 1 | 0 | 3 |
| 1 | 0 | 0 | 0 | 4 |
| 1 | 0 | 1 | 1 | 5 |
| 1 | 1 | 0 | 0 | 6 |
| 1 | 1 | 1 | 1 | 7 |

Implement the circuit via simulation software and paste the result in here

A computer diagram of a circuit board

Description automatically generated

Verify the truth table and make comment on the results

b.

Establish the truth table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| X | Y | Z | F | Num |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 2 |
| 0 | 1 | 1 | 0 | 3 |
| 1 | 0 | 0 | 0 | 4 |
| 1 | 0 | 1 | 1 | 5 |
| 1 | 1 | 0 | 0 | 6 |
| 1 | 1 | 1 | 1 | 7 |

Implement the circuit via simulation software and paste the result in here

A diagram of a circuit board

Description automatically generated

A diagram of a circuit board

Description automatically generated

A computer diagram of a circuit board

Description automatically generated

Verify the truth table and make comment on the results

𝒇 = 𝒙 ′𝒚𝒛 + 𝒙𝒚𝒛 + 𝒙𝒚 ′𝒛 + 𝒙𝒚𝒛 ′ + 𝒙𝒚 ′𝒛 ′ + 𝒙′𝒚′𝒛′